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# ΣΔ Modulator for Digital Wireless Architecture: A review

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***Abstract*— This paper studies Sigma-Delta (ΣΔ) technique to embed a complex modulation scheme such as orthogonal frequency division multiplexing (OFDM) into a single 'on'-'off' bit stream operating at the carrier frequency. The amplitude of the signal is related to the pulse widths and the phase to the pulse position. This paper concentrates on all digital upconverter structures of ΣΔ modulator architecture. The binary nature of their output removes the need for analog components in the up-conversion chain. Their outputs can be used directly to drive the switch mode power amplifier (SMPA) for high efficiency operation.**

## I. INTRODUCTION

Research in green communications is addressing energy efficiency of the telecommunications sector, to reduce the cost of emissions and the world's carbon footprint. Software-defined Radio (SDR) is gaining popularity because digital circuits provide software controllable features such as coding/decoding, modulation/demodulation, filtering, mixing, and power control [1-3]. The trend in SDR is to push the digital part close to the antenna part to remove analog selection mechanisms. However, traditional SDR still requires some analog components such as analog-to-digital and digital-to-analog converters (ADC/DAC), up/down converters, RF selectivity and RF amplification.

Digital wireless transmission is related to all-digital transmitter design with fully digital components. To move towards all-digital wireless transmitters, the elimination of analog components is required. Various signal processing innovations are now being proposed by the research community to this end. If such a solution can be found then integration on to low cost digital *Silicon* Complementary Metal Oxide Semiconductor (Si CMOS) technology will produce major reduction in both size, cost and energy consumption.

A traditional wireless transmitter architecture is described in Fig. 1 (top). It consists of analog components such as ADC/DAC, filters, a modulator (Mod), and a local oscillator (LO). A new wireless transmitter architecture in Fig. 1 (bottom) has introduced the use of a digital ΣΔ structure which replaces the analog components from the traditional transmitter architecture. Removal of the analog components also removes many analog problems, such as gain-phase imbalance and carrier leakage of the quadrature modulator, the need for an RF synthesiser and the need for wideband matching of the low-pass filters (LPF).

ΣΔ techniques are most well known for their use in ADC and DAC structures. These schemes are almost entirely based on the conversion of low-pass signals. The best known early application of ΣΔ DACs was for the compact disc (CD) player [4]. Here the sample rate was increased to reduce the (quantisation) noise power spectral density which was shaped by a first order filter to further reduce the noise in the lower frequencies. In this way high fidelity signal reproduction was possible from DAC's of reduced resolution.

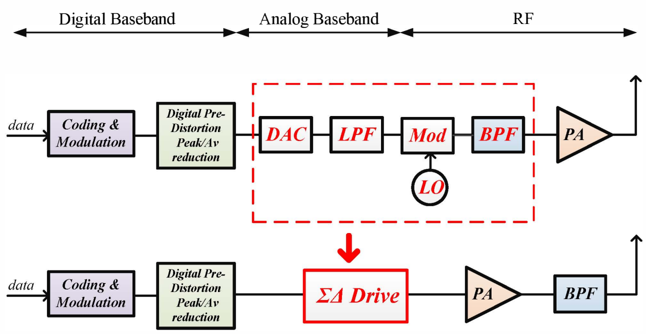


Figure 1. ΣΔ structure can potentially replace the analog components of the traditional wireless architecture (top). A potential future wireless transmitter architecture (bottom).

The study of ΣΔ modulator architecture is reviewed in this paper. Recent research is now applying ΣΔ techniques to band-pass signals such as found in radio frequency transceivers [5]. There are a number of challenges to developing such schemes. First, the carrier frequency is of the same order as the sample rate; secondly the bandwidth, EVM and spectral mask of any transmitted RF signal must be met; and thirdly, any design must be realisable in today's silicon technology. These three factors are all inter-related and form a complex trade-off between performance, complexity and energy consumption. This paper concentrates on all digital upconverter structures. The binary nature of their output removes the need for analog components in the up-conversion chain. Their outputs can be used directly to drive the SMPA (Class-S or Class-D) for high efficiency operation [6].

## II. BAND-PASS ΣΔ ARCHITECTURE

Band-pass ΣΔ modulator is proposed as a possible solution suitable for RF digital transmitter design using SMPA. A band-pass ΣΔ modulator generates a digital pulse train and shapes the quantisation noise which is then fed to the switched amplifier.

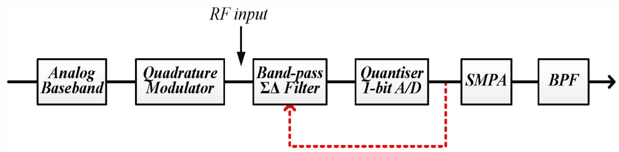


Figure 2. Band-pass ΣΔ Architecture in [6].

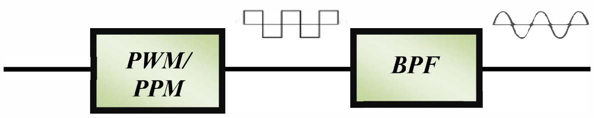


Figure 3. BPF for RF PWM/PPM output.

It is possible to avoid the analog processing by doing the up-conversion in DSP and replacing the band-pass ΣΔ 1-bit A/D with a band-pass ΣΔ 1-bit D/A as shown in Fig. 4 [7]. The DSP module generates the input signal as an *I* and *Q* baseband signal. The *I*-*Q* baseband is interpolated to a higher sampling frequency before digital up-conversion. The up-conversion operation multiplies the *I*-*Q* baseband signals with the pulse sequences of 1,1,-1,-1,… and -1,1,1,-1,… respectvely. The two signals are summed together and fed directly into the band-pass ΣΔ modulator, which generates the digital data streams for the SMPA. The band-pass ΣΔ transmitter architecture operates at a sampling frequency that is four times the RF carrier frequency. The high clock rate ($f_{clock}$) will require substantial power consumption which reduces efficiency [8] .

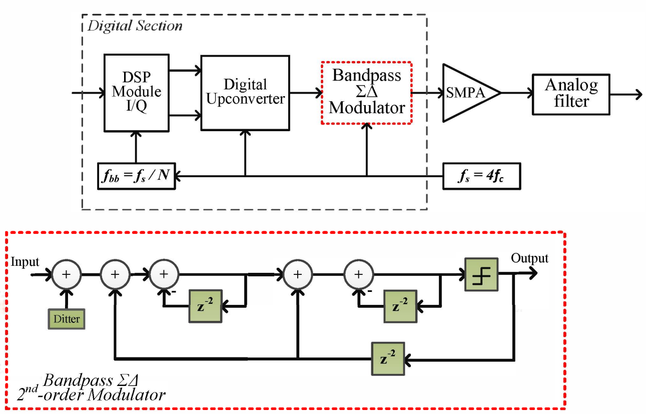


Figure 4. The band-pass ΣΔ (2nd order) architecture proposed in [7].

A digital method proposed in [9], implements the band-pass ΣΔ technique using a combination of two low-pass ΣΔ modulators and upconverters, Fig. 5. Each baseband *I* and *Q* signal has its own low-pass ΣΔ. The three multiplexer units (Mux) implement a quadrature modulator that up-converts the quantised one bit $\hat{I}$-$\hat{Q}$ signals to RF at a carrier frequency $f_c$.

$$y_{RF}(n) = \hat{Q}\sin\left(2\pi n\frac{f_c}{f_{clock}}\right) + \hat{I}\cos\left(2\pi n\frac{f_c}{f_{clock}}\right) \quad (1)$$

when $f_{clock} = 4f_c$ the above sequences become

$$\sin(2\pi n\frac{f_c}{f_{clock}}) = 0,1,0,-1,0,1,.... \quad (2)$$

$$\cos\left(2\pi n\frac{f_c}{f_{clock}}\right) = 1,0,-1,0,1,0 .... \quad (3)$$

The summation of the sequences is trivial and can be performed in a multiplexer (Mux), since one term is always 0.

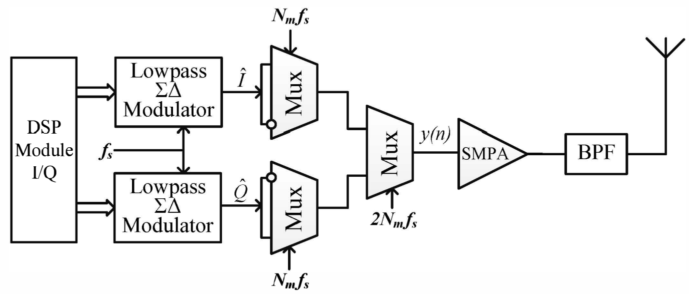


Figure 5. The band-pass ΣΔ (two low-pass ΣΔs) architecture proposed in [9].

It is possible to generate RF signals with carrier frequency $f_c > 1$ GHz using off-the-shelf multiplexer devices. However it is harder to achieve GHz sample rates ($f_s$) for the DSP and ΣΔ modulators without resorting to application-specific integrated circuit (ASIC) implementation [10]. The achievable bandwidth is proportional to sampling frequency $f_s$.

It is difficult to get high sampling rates on the ΣΔ D/A's because of the feedback path. The filtering and quantisation must all be completed within the latency of one clock period. Frappé *et al.* [11] developed an ASIC using Borrow-Save arithmetic, non-exact quantisation and a multiphase-clock to complete all calculations of a 3rd-order ΣΔ filter in 250 *ps* (pico second). A signal bandwidth of 50 MHz was obtained.

## III. Polar ΣΔ Architecture

Polar ΣΔ techniques operate on the polar (amplitude $A(t)$ and phase $\Phi(t)$) signals rather than the more normal *I*-*Q* representation. The polar ΣΔ structure was proposed in [12-15] where the aim was to reduce the switching activity and also to eliminate the need for analog components.

Fig. 6 shows a polar ΣΔ architecture consisting of a low-pass 1-bit ΣΔ modulator using a phase modulated clock and a gated PA [15]. The envelope input signal $A(t)$ represents the average value of the 'on'-'off' period of the square wave signal at the output of the low-pass ΣΔ modulator. The phase information is represented by the zero-crossing timing of the RF carrier. The PA is operated in saturated mode (for best performance with a Class-C structure [16]), and the input waveforms are square waves. This scheme implements burst-mode modulation where the ΣΔ modulator switches the square wave RF input signal 'on' or 'off' [15].

Keyzer *et al.* in [13], the architecture consists of the two ΣΔ modulators (each modulator generates a pulse train representing the phase and amplitude signals respectively), followed by up-conversion blocks to perform PWM and PPM generation, Fig. 7. The amplitude is quantised into three


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levels and the phase is quantised into eight levels. A digital pulse delay modulator acts on an input periodic pulse train with period of $f_c$ and pulse width $\frac{1}{8f_c}$ to produce an output phase modulated pulse train. This is then followed by a pulse expander to change the phase width. The structure limits the number of pulses per period to one and there is often no switching pulse when the input signal is small. Therefore, it should have good efficiency; however there is a bandwidth penalty.

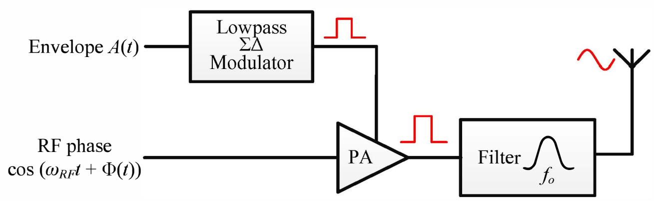


Figure 6. The polar ΣΔ based burst-mode architecture proposed in [15].

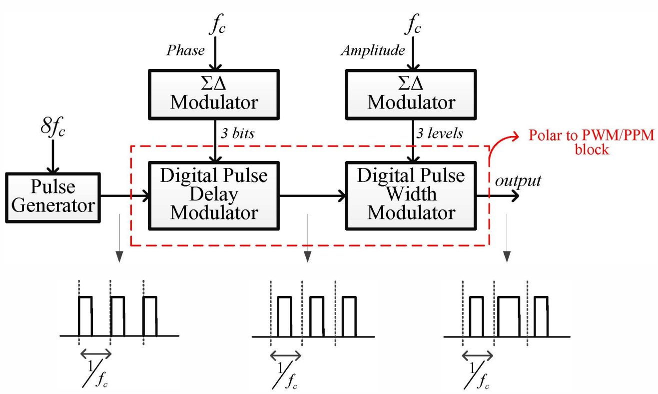


Figure 7. The polar ΣΔ architecture proposed in [13].

Bassoo *et al.* in [14] investigated the polar ΣΔ structure which is shown in Fig. 8. The input signal of *I-Q* complex baseband is converted to polar representations, $R = \sqrt{I^2 + Q^2}$ and $\theta = \tan^{-1}\left(\frac{Q}{I}\right)$ . Low-pass ΣΔ's are used to independently quantise the $R$ (amplitude) and the $\theta$ (phase) signals respectively. The $R$ value is quantized into 4 distinct levels while $\theta$ is quantized to 16 levels uniformly distributed between 0 to $2\pi$. The output of these quantisers is fed back to their appropriate ΣΔ filter. The quantized signal is also passed through to a 'Polar to PWM/PPM' block converter to generate the appropriate pulse waveform. The pulse train output of the 'Polar to PWM/PPM' block feeds to the SMPA and BPF.

Normally, the ΣΔ filters update the pulse width and position every whole number of cycles of the carrier frequency (or half cycles if a bridge amplifier is used). The ΣΔ filters for the phase signal must be modified to handle the phase wrap-around. The polar components have a wider bandwidth than the *I-Q* components, and this limits the modulation bandwidth of this structure hence the effective oversampling rate is reduced. Besides that, the conversion process of *I-Q* complex baseband from Cartesian format to polar format is a nonlinear process which causes some of the quantisation noise to fold back into the band of interest and hence it cannot be filtered out [17].

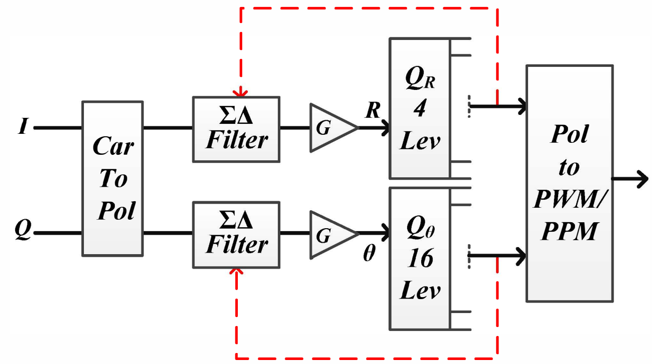


Figure 8. Polar ΣΔ Architecture proposed in [14].

Another problem is unwanted spectral components which arise when baseband polar signals are upconverted to RF using PWM/PPM techniques. The 'Polar to PWM/PPM' block upconverts the signal to RF with quantised amplitude and phase. The amplitude of the RF is controlled by the pulse width and the phase of the RF is controlled by the pulse position. In the PPM process, a change in phase is represented by a change in position and the pulse edge must occur on the digital timing grid. This process eventually leads to amplitude modulation (AM) as a pulse is swallowed whenever there is a change in quantisation level. Recently, Bassoo *et al.* in [14] has established that the dominant distortions are the image and harmonic components generated in the PPM circuit ('Polar to PWM/PPM' block).

## IV. Cartesian ΣΔ Architecture

The authors in [18, 19] realised that Cartesian ΣΔ upconverters are an improvement over the polar ΣΔ modulator in [14], with regard to solving the bandwidth expansion problems and reducing switching activity. Fig. 9 shows the comparison plot between polar and Cartesian ΣΔs using an OFDM signal. The output spectrum and ACP versus signal level are compared. The Cartesian ΣΔ has better noise shaping with a better null around the band of interest and lesser noise than the polar ΣΔ (Fig. 10(a)). Fig. 10(b) shows the Cartesian ΣΔ has at least 10 dB less ACP, over a wide dynamic range of input signal levels, compared to the polar ΣΔ.

The proposed Cartesian ΣΔ structure can be seen in Fig. 10. It consists of MOD2 low-pass ΣΔs [4] for the Cartesian $I$ and $Q$ input signals. After ΣΔ-filtering, the $I$ and $Q$ signals are then converted to polar co-ordinates [$R$, $\theta$] and separately quantised in the $Q_R$ and $Q_\theta$ blocks resulting into $[\hat{R}, \hat{\theta}]$. The Gain block (normally set to G ≤ 1) works to improve efficiency (by reducing the number of switching edges) at the expense of a degraded spectrum [20]. The output of the quantisers is converted back to Cartesian co-ordinates, $[\hat{I}, \hat{Q}]$ (removing bandwidth expansion [20]) and fed as feedback to the ΣΔ filters. The outputs of both quantisers are also


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upconverted to RF using PWM/PPM techniques in the 'Polar to PWM/PPM' block.

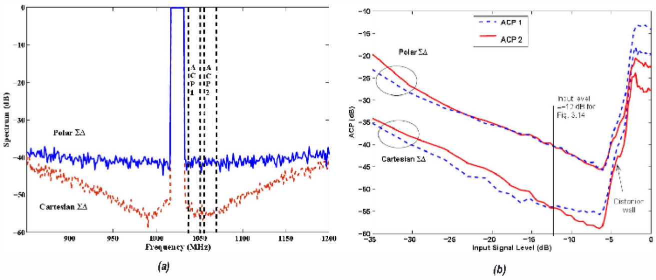


Figure 9. (a) Normalized spectrum of OFDM and (b) ACP for Cartesian ΣΔ and polar ΣΔ modulator [18].

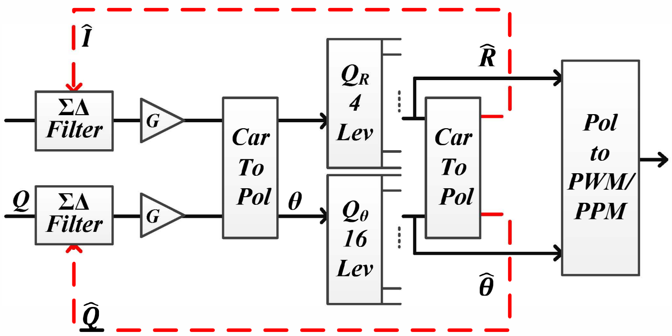


Figure 10. Cartesian ΣΔ Architecture [21]. ΣΔ filtering is in Cartesian with quantisation in polar.

The proposed quantiser used an even quantisation technique where the three-level-waveform at the output is based on pulses with an even number of clock periods [18, 21, 22]. The quantised amplitudes, $\hat{R}$, of the RF signal are calculated by changing the pulse widths in increments of two clock periods. However, this leads to a potential coarse quantisation at low signal levels, as the minimum pulse width in the even quantisation scheme is two clock periods.

Furthermore, while reducing the bandwidth expansion, the Cartesian ΣΔ model may still cause unwanted spectral components due to the 'Polar to PWM/PPM' block. The most relevant work to the aims of the proposed research was presented in [21]. It showed that in a single carrier environment, an increase in offset frequency increases the unwanted spectral components. The image and 3rd order harmonic components are the dominant distortions. The PPM block was shown to be responsible for these distortions, but no solutions were proposed.

## V. Conclusion

RF up-conversion using ΣΔ techniques is a potential replacement to traditional techniques using analog circuits. The all-digital output creates a number of noise and distortion products. Techniques to address these problems have been discussed.

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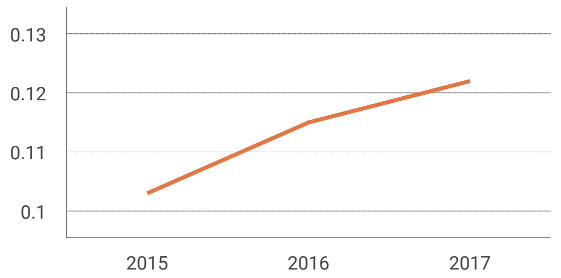


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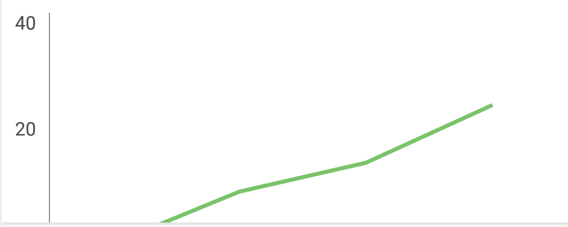


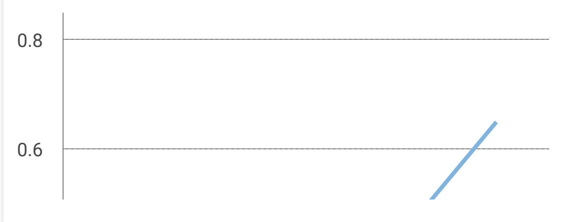


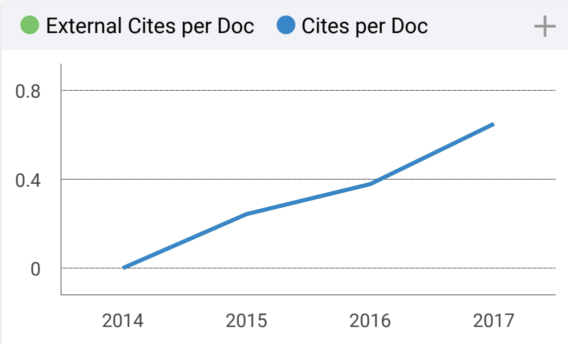


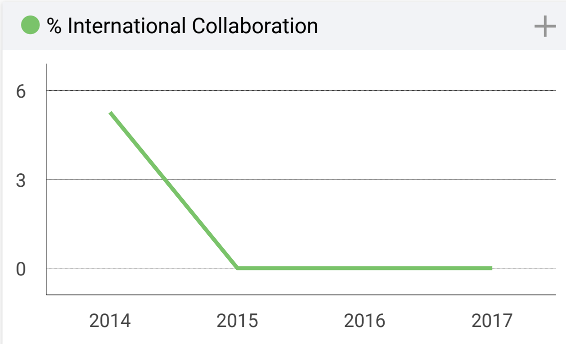


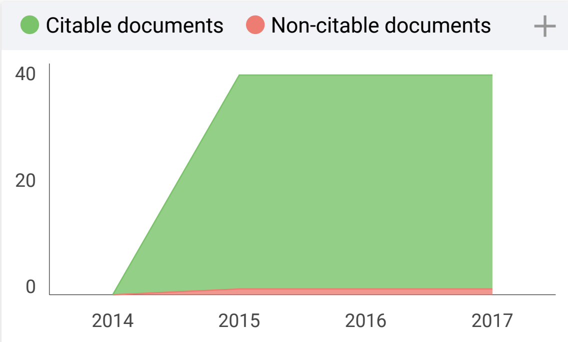


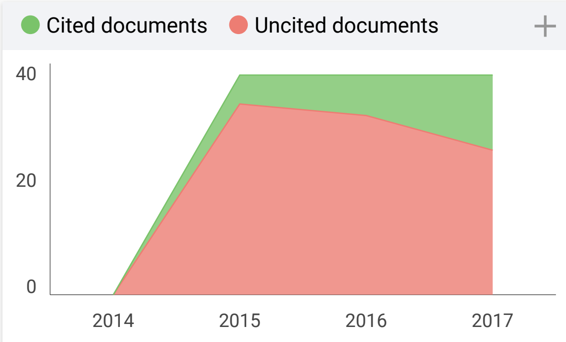



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